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IC SPI P
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NCN6804

The NCN6804 is a dual interface IC with serial control. It is dedicated for Smart Card/Secure Access Module (SAM) reader/writer applications. It allows the management of two external ISO/EMV cards (Class A, B or C). An SPI bus is used to control and configure the dual interface. The cards are controlled in a multiplexed mode. Two NCN6804 devices (4 smart card interfaces) can share one single control bus thanks to a dedicated hardware address pin (S1).

An accurate protection system guarantees timely and controlled shutdown in the case of external error conditions.

This device is an enhanced version of the NCN6004A, more compact, more flexible and fully compatible with the NCN6001, its single interface counterpart version. It is fully compatible with ISO 7816 3, EMV and GIE CB standards.

Features

Dual Smart Card / SAM Interface with SPI Programming Bus

Fully Compatible with ISO 7816 3, EMV and GIE CB Standards

One Protected Bidirectional Buffered I/O Line per Card Port

Wide Power Supply Voltage Range: $2.7V < V_{DDPA/B}$ & $V_{DD} < 5.5$ V

Programmable/Independent CRD_VCC Supply for Each Smart Card

Multiplexed Mode of Operating
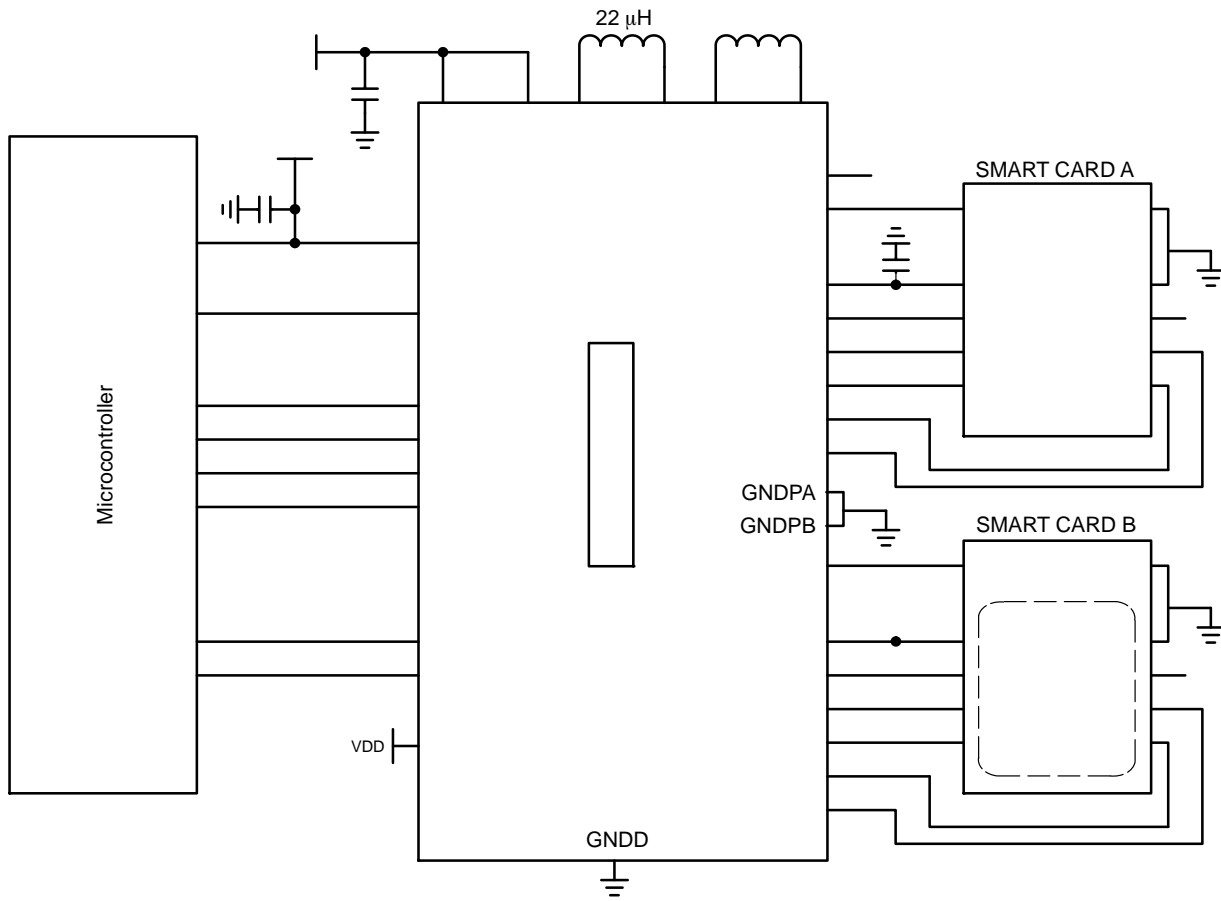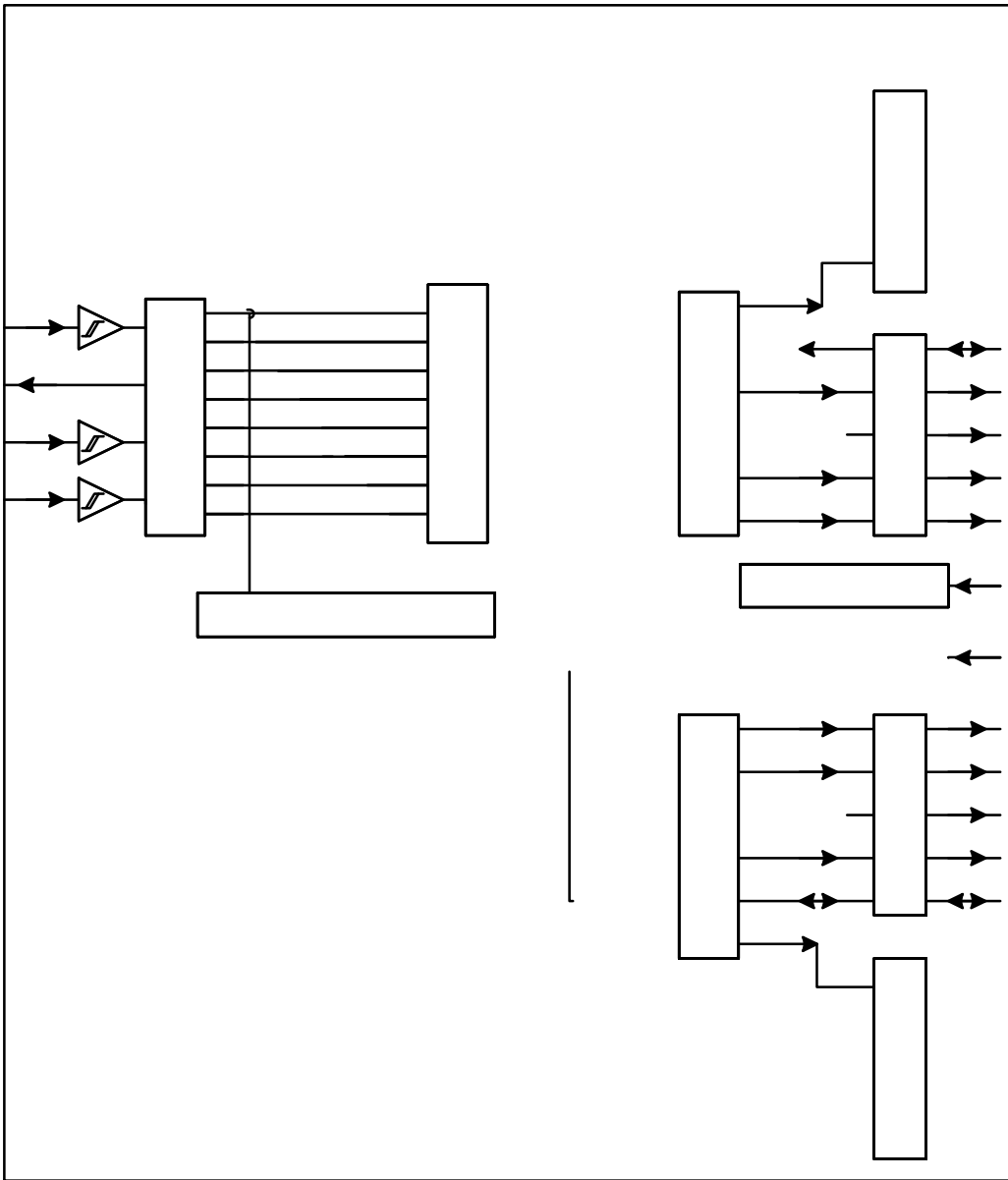
Handles 1.8 V, 3.0 V and 5.0 V Smart Cards

NCN6804

22 μH

Microcontroller

SMART CARD A

SMART CARD B

GNDPA
GNDPB

VDD

GNDD

Figure 1. Typical Interface Application

PIN FUNCTION AND DESCRIPTION

PIN	Name	Type	Description
1	S1	I	Address pin (Chip Identification pin) – allows having in parallel up to 2 NCN6804 devices (4 interfaces) managed by 1 Chip Select pin only ($\overline{CS}$) – multiple interface application case. When one dual interface only is used this pin can be connected to GROUND.
2, 23	CRD_DETA, CRD_DETB	I	The signal coming from the external card connector is used to detect the presence of the card. A built in pull up low current source biases this pin HIGH, making it active LOW, assuming one side of the external switch is connected to ground. A built in digital filter protects the system against voltage spikes present on this pin. The polarity of the signal is programmable by the MOSI message; refer to Table 2. On the other hand, the meaning of the feedback message contained in the MISO register bit b4, depends upon the SPI mode of operation as defined here below: SPI Normal Mode: The MISO bit b4 is HIGH when a card is inserted, whatever be the polarity of the card detect switch. SPI Special Mode: The MISO bit b4 copies the logic state of the card detect switch as depicted here below, whatever be the polarity of the switch used to handle the detection: CRD_DET = LOW => MISO/b4 = LOW CRD_DET = HIGH => MISO/b4 = HIGH In both cases, the chip must be programmed to control the right logic state (Table 2). Since the bias current supplied by the chip is very low, typically 5.0 μ

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PIN FUNCTION AND DESCRIPTION

PIN	Name	Type	Description
25	I/O	I/O	This pin is connected to an external micro controller (μC) interface. A bi directional level translator adapts the serial I/O signal between the smart card and the μC. The level translator is enabled when $\overline{CS}$ = LOW, the sub address has been selected and the system operates in the Asynchronous mode. When a Synchronous card is in use this pin is disconnected and the data and transaction take place through the MOSI and the MISO registers. The internal pull up resistor connected on the μC side is activated and visible by the selected chip only.

MAXIMUM RATINGS (Note 3)

Rating	Symbol	Value	Unit
DC/DC Converter Power Supply Voltage ($V_{DDPA/B}$)	V_{sup} (Note 4)	$0.5 \leq V_{sup} \leq 6$	V
Power Supply from Microcontroller Side (V_{DD})	V_{DD}	$0.5 \leq V_{DD} \leq 6$	V
External Card Power Supply (Card A and B)	CRD_VCC	$0.5 \leq CRD\_VCC \leq 6$	V
Digital Input Pins	V_{in} I_{in}	$0.5 \leq V_{in} \leq (V_{DD} + 0.5)$ but < 6.0 5	V mA
Digital Output Pins (I/O, MISO, $\overline{INT}$)	V_{out} I_{out}	$0.5 \leq V_{out} \leq (V_{DD}+ 0.5)$ but < 6.0 10	V mA
Smart Card Output Pins	V_{out}	$0.5 \leq V_{out} \leq (CRD\_VCC + 0.5)$ but < 6.0	V
Smart Card Output Pins Excepted CRD_CLK	I_{out}	15 (Internally Limited)	mA
CRD_CLK Pin	I_{out}	70 (Internally Limited)	mA
Inductor Current	I_{Lmax}	500 (Internally Limited)	mA
QFN 32 5x5 mm^2 package Power Dissipation @ T_A = +85 C Thermal Resistance Junction to Air	P_D $R_{\theta jA}$	1650 40	mW C/W

POWER SUPPLY SECTION (40 C to +85 C, unless otherwise noted)

Pin	Symbol	Rating	Min	Typ	Max	Unit
12, 13	I					

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DIGITAL INPUT/OUTPUT SECTION CLK_IN, I/O, CLK_SPI, MOSI, MISO, $\overline{CS}$, $\overline{INT}$, EN_RPU (40 C to +85 C)

Pin	Symbol	Rating	Min	Typ	Max	Unit
26	F_{CLK_IN}	Input Asynchronous Clock Duty Cycle = 50% @ V_{DD} = 3.0 V @ V_{DD} = 5.0 V			30 40	MHz
26	F_{tr} F_{tf}	Input Clock Rise time Input Clock Fall time	2 2			ns
28	F_{CLK_SPI}	Input SPI clock			15	MHz
28	tr_{spi}, tf_{spi}	Input CLK_SPI Rise/Falltime			12	ns
30	tr_{mosi}, tf_{mosi}	Input MOSI Rise/Falltime			12	ns
29	tr_{miso}, tf_{miso}	Output MISO Rise/Falltime @ C_S = 30 pF			12	ns

SMART CARD INTERFACE SECTION (40 C to +85 C temperature range unless otherwise noted)
Note: Digital inputs undershoot ≤ 0.30V to ground, digital inputs overshoot < V_{DD} + 0.30V

Pin	Symbol	Rating	Min	Typ	Max	Unit

6,19	V_{OH}
	V_{OL}
	
	t_R
	t_F
		CRD_RSTA/B @ CRD_VCCA/B = 1.8 V, 3.0 V, 5.0 V
		    Output RESET V_{OH} @ I_{rst} = 200 µA
		    Output RESET V_{OL} @ I_{rst} = 200 µA
		CRD_RSTA/B @ CRD_VCCA/B = 1.8 V, 3.0 V, 5.0 V
		Output RESET Risetime @ C_{out} = 30 pF
		Output RESET Falltime @C_{out} = 30 pF
			CRD_VCC – 0.5		CRD_VCC
					0.40
					
					100
					100
						V
						V
						
						ns
						ns

3, 4
21, 22
	V_{OH}
	V_{OL}
	t_R
	t_F
		CRD_C4A/B, CRD_C8A/B
		    @ CRD_VCCA/B = 1.8 V, 3.0 V, 5.0 V
		    Output V_{OH} @ I_{rst} = 200 µA
		    Output V_{OL} @ I_{rst} = 200 µA
		Output Rise time @ C_{out} = 30 pF
		Output Fall time @C_{out} = 30 pF
			CRD_VCC 0.5		CRD_VCC
					0.4
					100
					100
						V
						V
						ns
						ns

7, 18	F_{CRDCLK}
	V_{OH}
	V_{OL}
	
	F_{CRDDC}
	
	t_{ress}
	t_{fcs}
	
	t_{rills}
	t_{ulsa}
		CRD_CLKA/B as a function of CRD_VCCA/B
		
		CRD_VCCA/B = 1.8 V, 3.0 V or 5.0V
		    Output Frequency
		    Output V_{OH} @ Icrd_clk = 200µA
		    Output V_{OL} @ Icrd_clk = 200µA
		
		CRD_CLKA/B Output Duty Cycle
		    CRD_VCCA/B = 1.8 V, 3.0 V or 5.0 V
		
		Rise & Fall time
		@ CRD_VCCA/B = 1.8 V, 3.0 V or 5.0 V
		Clock programmed as FST_SLP
		    Output CRD_CLKA/B Risetime @ C_{out} = 30 pF
		    Output CRD_CLKA/B Falltime @ C_{out} = 30 pF
		
		Rise & Fall time @ CRD_VCCA/B = 1.80V to 5.0V
		Clock programmed as SLO_SLP
		    Output CRD_CLKA/B Risetime @ C_{out} = 30 pF
		    Output CRD_CLKA/B Falltime @ C_{out} = 30 pF
			CRD_VCC 0.5
			
			45
					20
					CRD_VCC
					0.4
					
					55
					
					4
					4
					
					16
					16
						MHz
						V
						V
						
						%
						
						ns
						ns
						
						ns
						ns

5,20	V_{IH} V_{IL} V_{OH} V_{OL} t_R t_F	CRD_IOA/B Input Voltage High Level @ CRD_VCCA/B = 1.8 V, 3 V and 5 V CRD_IOA/B Input Voltage Low Level @ CRD_VCCA/B = 1.8 V, 3 V and 5 V Output V_{OH} @ Icrd_I/O = 20µA, V_{IH} = VDD @ CRD_VCCA/B = 1.8 V, 3 V and 5 V Output V_{OL} @ Icrd_I/O = 500 µA, V_{IL} = 0 V @ CRD_VCCA/B = 1.8 V, 3 V and 5 V CRD_IOA/B Rise Time, @ C_{out} = 30 pF CRD_IOA/B Fall Time, @ C_{out} = 30 pF	CRD_VCC*0.6 0.30 CRD_VCC – 0.5 0		CRD_VCC+0.3 0.80 CRD_VCC 0.40 0.8 0.8	V V V V V µs µs
5, 20	R_{CRDPU}	CRD_IOA/B Pull Up Resistor	12	18	24	kΩ

2, 23	T_{CRDIN}
	T_{CRDOFF}
		Card Detection digital filter delay:
		    Card Insertion
		    Card Extraction
			25
			25
				50
				50
					150
					150
						µs
						µs

2, 23	V_{IHDET}	Card Insertion or Extraction Positive going Input High Voltage	0.70 * VCC		VCC	V
2, 23	V_{ILDET}	Card Insertion or Extraction Negative going Input Low Voltage	0		0.30 * VCC	V

SMART CARD INTERFACE SECTION (40 C to +85 C temperature range unless otherwise noted)

Note: Digital inputs undershoot $\leq$ 0.30V to ground, digital inputs overshoot < V_{DD} + 0.30V

Pin	Symbol	Rating	Min	Typ	Max	Unit
3, 4, 5, 6, 19, 20, 21, 22	Icrd	Output peak Max Current under Card Static Operation Mode @ CRD_VCC = 1.8V, 3.0V, 5.0V CRD_I/OA/B, CRD_RSTA/B, CRD_C4A/B, CRD_C8A/B			15	mA
7, 18	Icrd_clk	Output peak Max Current under Card Static Operation Mode @ CRD_VCC = 1.8 V, 3.0 V, 5.0 V CRD_CLKA/B			70	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

PROGRAMMING
Write Register → WRT_REG (Is Low Only)

Similar to the NCN6001, the NCN6804's WRT_REG register handles 3 command bits [b5:b7] and 5 data bits [b0:b4] as depicted in Tables 1 and 2. These bits are concatenated into 1 byte [MSB0,LSB0] in order to accelerate the programming sequence. The register can be updated when $\overline{CS}$ is low only.

The WRT_RGT has been defined to be compatible with the NCN6001 write register.

Table 1. WRT_REG BIT DEFINITIONS

b0
b1
	If (b7 + b6 + b5) = 000 or (b7 + b6 + b5) = 010 then
	        Case 00
	                CRD_VCCA = 0 V
	        Case 01
	                CRD_VCCA = 1.8 V
	        Case 10
	                CRD_VCCA = 3.0 V
	        Case 11
	                CRD_VCCA = 5.0 V
	Else if (b7 + b6 + b5) = 001 or (b7 + b6 + b5) = 011 then
	        Case 00
	                CRD_VCCB = 0 V
	        Case 01
	                CRD_VCCB = 1.8 V
	        Case 10
	                CRD_VCCB = 3.0 V
	        Case 11
	                CRD_VCCB = 5.0 V
	Else if (b7 + b6 + b5) =110 or (b7 + b6 + b5) = 111 then
	        b1 drives CRD_C4A or B (respectively)
	        b0 drives CRD_C8A or B (respectively)
	Else if (b7 + b6 + b5) =101 then
	        Case 00
	                CRD_DET = NO
	        Case 01
	                CRD_DET = NC
	         Case 10
	                SPI_MODE = Special
	        Case 11
	                SPI_MODE = Normal
	Else if (b7 + b6 + b5) =100 then
	        NA (Not Applicable)
	End if

8. When operating in Asynchronous mode, b6 is compared with the external voltage level present pin S1 (Pin 1).
9. The CRD_RST pin reflects the content of the MOSI WRT_REG [b4] during the chip programming sequence. Since the bit shall be Low to address the chip's internal register, care must be observed as this signal will be immediately transferred to the CRD_RST pin.

Table 1. WRT_REG BIT DEFINITIONS

b2
b3
	If (b7 + b6 + b5) = 000 or (b7 + b6 + b5) = 010 then
	        Case 00
	            CRD_CLKA = Low
	        Case 01
	           CRD_CLKA = CLK_IN
	        Case 10
	           CRD_CLKA = CLK_IN / 2
	        Case 11
	           CRD_CLKA = CLK_IN / 4
	
	Else if (b7 + b6 + b5) = 001 or (b7 + b6 + b5) = 011 then
	        Case 00
	           CRD_CLKB = Low
	        Case 01
	           CRD_CLKB = CLK_IN
	        Case 10
	           CRD_CLKB = CLK_IN / 2
	        Case 11
	           CRD_CLKB = CLK_IN / 4
	
	Else if (b7 + b6 + b5) =110 or (b7 + b6 + b5) = 111 then
	        b3 drives CRD_CLKA or B (respectively)
	        b2 drives CRD_IOA or B (respectively)
	Else if (b7 + b6 + b5) =101 then
	        Case 00
	           CRD_CLKA & B = SLO_SLP
	        Case 01
	           CRD_CLKA & B = FST_SLP
	        Case 10
	           NA
	        Case 11
	           NA
	Else if (b7 + b6 + b5) =100 then
	        NA (Not Applicable)
	End if

b4	If (b7 + b6 + b5) <> 101 and (b7 + b6 + b5) <> 100 then b4 Drives CRD_RSTA or B Pin
b5 b6 b7	000 Select NCN6804 device # 1 Asynchronous Card A (Note 8) 001 Select NCN6804 device # 1 Asynchronous Card B (Note 8) 010 Select NCN6804 device # 2 Asynchronous Card A (Note 8) 011 Select NCN6804 device # 2 Asynchronous Card B (Note 8) 100 NA 101 Set Card Detection Switch polarity, Set SPI_MODE normal or special , Set CRD_CLKA & B slopes Fast or Slow 110 Select External Synchronous Card A 111 Select External Synchronous Card B

8. When operating in Asynchronous mode, b6 is compared with the external voltage level present pin S1 (Pin 1).
9. The CRD_RST pin reflects the content of the MOSI WRT_REG [b4] during the chip programming sequence. Since the bit shall be Low to address the chip's internal register, care must be observed as this signal will be immediately transferred to the CRD_RST pin.

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Table 2. WRT_REG BIT DEFINITIONS AND FUNCTIONS

ADRESS								MOSI bits[b3 : b2]	MOSI bits [b1 : b0]	MOSI bits [b3 : b0]
MSB0					LSB0			CRD_CLK	CRD_VCC	
b7	b6	b5	b4	b3	b2	b1	b0			
0	S1	A/B	CRD_RST	0	0	0	0	Low	0	
0	S1	A/B	CRD_RST	0	1	0	1	1/1	1.8V	
0	S1	A/B	CRD_RST	1	0	1	0	1/2	3.0V	
0	S1	A/B	CRD_RST	1	1	1	1	1/4	5.0V	
1	1	A/B	CRD_RST	CRD_CLK	CRD_I/O	CRD_C4	CRD_C8			Synchronous
1	0	1	X	X	0	0	0			NO
1	0	1	X	X	0	0	1			NC
1	0	1	X	X	0	1	0			Special
1	01	1	X	X	0	1	1			Normal

Read Register → READ_REG

The READ_REG register (1 byte) contains the data read from the card interface. The selected chip register is transferred to the MISO Pin during the MOSI sequence ($\overline{CS}$ = Low).

Table 3 gives a definition of the bits.

Depending upon the programmed SPI_MODE, the content of READ_REG is transferred on the MISO line either on the Positive going (SPI_MODE = Special) or upon the Negative going slope (SPI_MODE = Normal) of the CLK_SPI signal.

The external microcontroller shall discard the three high bits since they carry no valnoFnI_MO0009 Tc[7ata read

Asynchronous Mode

In this mode, the S1 pin is used to define the physical address (by comparison with the bit b6 (MOSI)) of the interfaces when a bank of up to 2 NCN6804 (total of 4 interfaces) shares the same digital bus.

Synchronous Mode

In this mode, the CLK_IN clock input and the I/O input/output are not used. The clock and the data are provided and transferred through the SPI bus using MOSI and MISO as shown Table 2.

When this operating mode is used and if two NCN6804 devices want to be implemented, it is no longer possible to share the same $\overline{CS}$ signal. Consequently in this particular case and when the devices operate in a multiple interface mode a dedicated $\overline{CS}$ signal must be provided to each NCN6804 device.

Since bits [b4 – b0] of the MOSI register contain the smart card data, programming the CRD_VCC output voltage shall be done by sending a previous MOSI message according to Table 2 using the address [b7, b6, b5] = [0, S1, A/B]. For example if a synchronous card is used, prior to make a transaction with it, it will be powered up for example at 5 V by sending the command %00000011 (address S1 = 0 and card A selected).

The CRD_RSTA/B pin reflects the content of the MOSI WRT_REG [b4] during the chip programming sequence. Since this bit shall be LOW to address the internal register of the chip, care must be observed as this signal will be immediately transferred tot he CRD_RSTA/B pin.

Startup Default Conditions

At startup, when power supply is turned on, the internal POR (Power On Reset) circuit sets the chip in the default conditions as defined below (Table 4).

Table 4. STARTUP DEFAULT CONDITIONS

CRD_DETA/B	Normally Open
CRD_VCCA/B	OFF
CRD_CLKA/B	tr & tf = SLOW
CRD_CLKA/B	LOW
Protocol	Special Mode
I/O Pull up resistor	Connected
$\overline{INT}$	High

Card Detection

The card is detected by the external switch connected to pin 23 for Card B and pin 2 for Card A. The internal circuit provides a positive bias of this pin and the polarity of the insertion/extraction is programmable by the MOSI protocol as depicted Table 2.

The bias current is 1μ
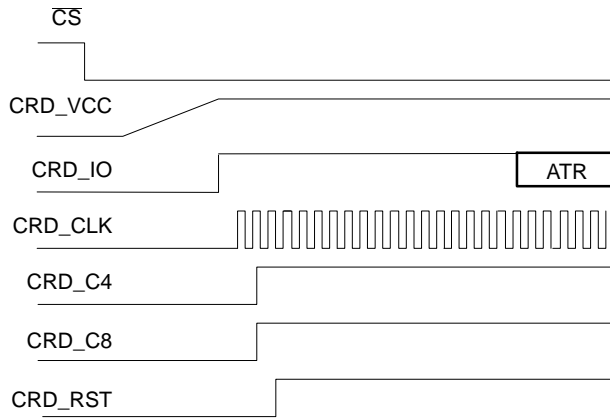
Figure 3. Startup CRD_VCC Sequence
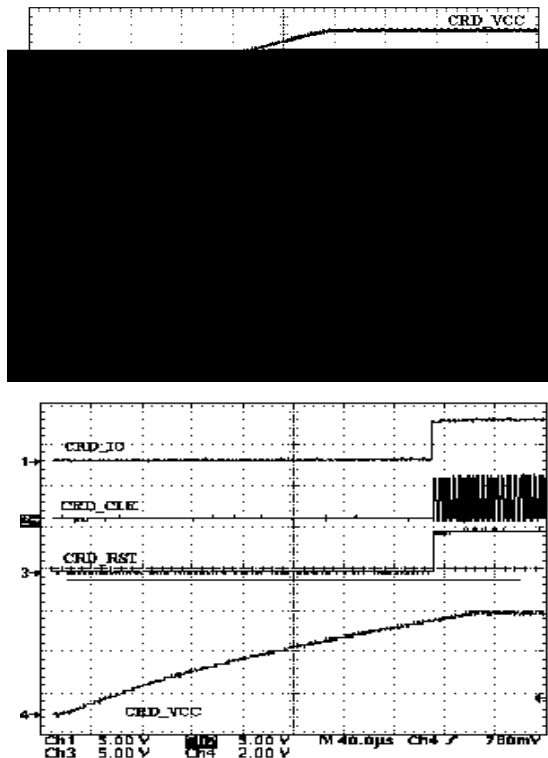
Figure 4. Measured Typical Startup CRD_VCC Sequence

At powerup, the CRD_VCCA/B turn on time depends upon the current capability of the DC/DC converter associated with the external inductor L and the reservoir capacitor connected across CRD_VCCA or B and GROUND. During this sequence, the average input current is 300 mA typical (see Figure 4), assuming the system is fully loaded during the start up.

Even if enabled by the built in sequencer the activation sequence is under the control and responsibility of the application software.

On the other hand, at turn off, the CRD_VCCA/B fall time depends upon the external reservoir capacitor and the peak current absorbed by the internal NMOS transistor built across CRD_VCCA/B and Ground. These behaviors are depicted Figure 5.

Since these parameters have finite values, depending upon the external constraints, the designer must take care of these limits if the t_{ON} or t_{OFF} provided by the datasheet does not meet his requirements.
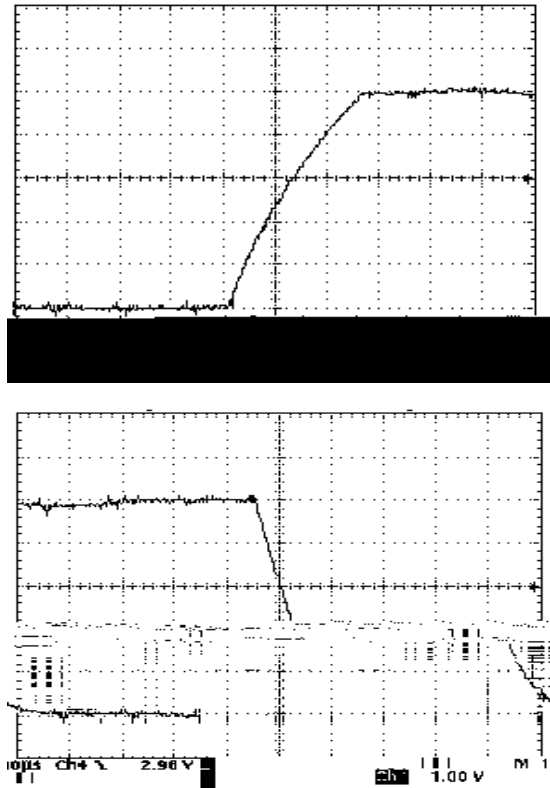
Figure 5. CRD_VCC Typical Turn−on and Turn−off Times

Figure 6. Figure 7: Start Up Sequence with ATR.

Figure 7. Typical Power Down Sequence
(Typical Delay Between Each Signal is 500 ns)

Powerdown Sequence

The NCN6804 provides an automatic Power Down sequence, according to the ISO7816 3 specifications. When a power down sequence is enabled the communication session terminates immediately. The sequence is launched under a micro controller decision, when the card is extracted, or when the CRD_VCCA/B voltage is overloaded as described by the ISO/CEI 7816 3 sequence depicted here after (see Figure 8):

→ CRD_ RST is forced to Low

→ CRD_CLK is forced to Low, unless it is already in this state

→ CRD_C4 & CRD_C8 are forced to Low

→ Then CRD_IO is forced to Low

→ Finally the CRD_VCC supply is powered down

Since the internal digital filter is activated for any card insertion or extraction, the physical power down sequence will be activated 50 µs (typical) after the card has been extracted. Of course, such a delay does not exist when the micro controller intentionally launches the power down.

Data I/O Level Shifter

The level shifter accommodates the voltage difference that might exist between the micro controller and the smart card. A pulsed accelerator circuit provides the fast positive going transient according to the ISO7816 3 specifications. The basic I/O level shifter is depicted Figure 8.

Table 7. INTERRUPT RESET LOGIC TABLE

Interrupt Source ($\overline{INT}$ set to LOW)	$\overline{CS}$	Interrupt Clearance ($\overline{INT}$ reset to HIGH) CRD_VCCA/B / {b1, b0} Programming	Chip Address
Card Insertion	L	{0,1}, {1,0} or {11}	{b7:b5} = 0XX
Card Extraction	L	{0,0}	{b7:b5} = 0XX
Over Load	L	{0,0}	{b7:b5} = 0XX

In order to know the source of the interrupt (card A or card B), the software has to poll the MISO register by sending a MOSI A command (address {b7, b6, b5} = {0, X, 0}) followed by a MOSI B command (address {b7, b6, b5} = {0, X, 1}) (or conversely). The corresponding MISO content provides the previous state of the interface A or B that is the information related to the cause of the interrupt. For each case the MISO status obtained will be compared with the MISO state prior to the interrupt. When 2 NCN6804 devices share the same digital SPI bus, it is up to the software to poll the devices using again the MISO register to identify the reason of the interrupt.
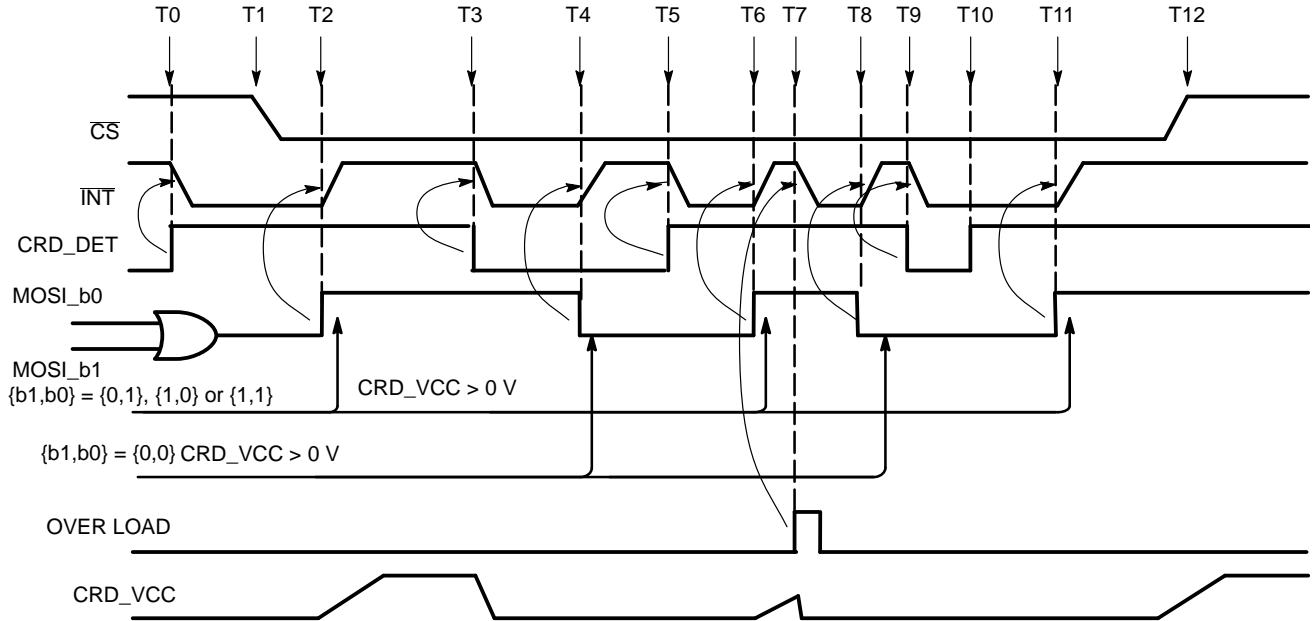
Figure 10. Basic Interrupt Function

SPI Port

The product communicates to the external micro controller by means of a serial link using a Synchronous Port Interface protocol, the CLK_SPI being Low or High during the idle state. The NCN6804 is not intended to operate as a Master controller, but executes commands coming from the MPU.

The CLK_SPI, $\overline{\text{CS}}$ and MOSI signals are under the microcontroller's responsibility. The MISO signal is generated by the NCN6804, using the CLK_SPI and CS lines to synchronize the bits carried out by the data byte. The basic timings are given in Figure 11 and 12. The system runs with two internal registers associated with MOSI and MISO data:

WRT_REG is a write only register dedicated to the MOSI data.

READ_REG is a read only register dedicated to the MISO data.
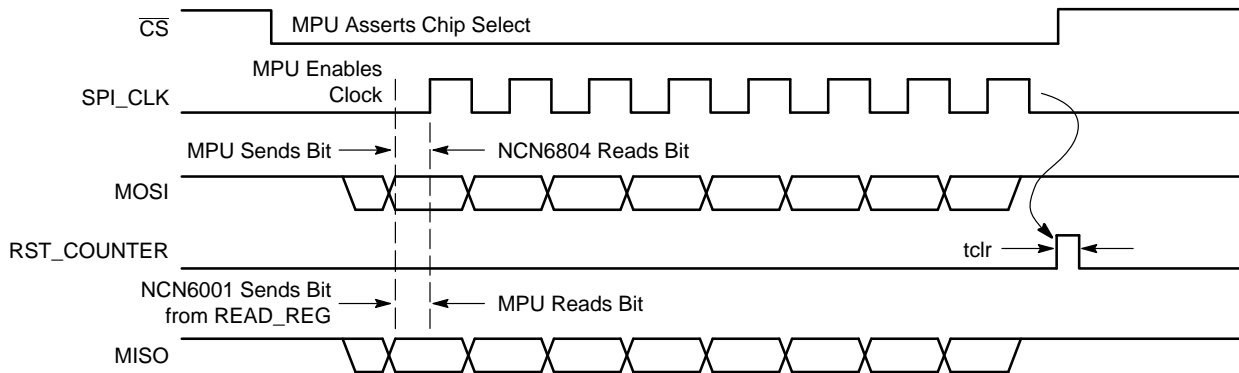
Figure 11. Basic SPI Timings and Protocol

When the $\overline{\text{CS}}$ line is High, no data can be written or read on the SPI port. The two data lines become active when $\overline{\text{CS}}$ = Low, the internal shift register is cleared and the communication is synchronized by the negative going edge of the $\overline{\text{CS}}$ signal. THe data presents on the MOSI line are considered valid on the negative going edge of the CLK_SPI clock and is transferred to the shift register on the next positive edge of the same CLK_SPI clock.

To accommodate the simultaneous MISO transmit, an internal logic identifies the chip address on the fly (reading and decoding the three first bits) and validate the right data present on the line. Consequently, the data format is MSB first to read the first three signal as bits b5, b6 and b7. The chip address is decoded from this logic value and validates the chip according to the S1 pin conditions: see Figure 12.
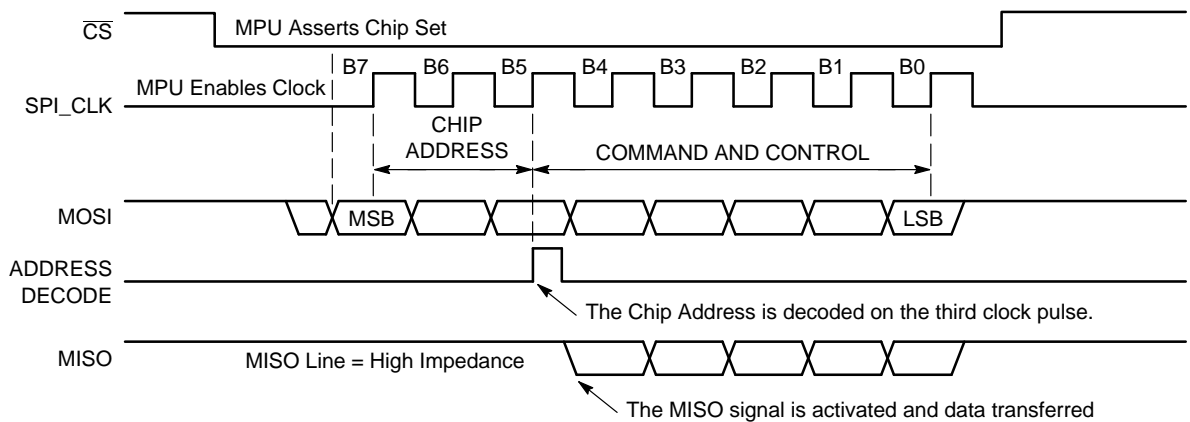
Figure 12. Chip Address Decoding Protocol and MISO Sequence

When the bit transfer is completed, the content of the internal shift register is latched on the positive going edge of the $\overline{\text{CS}}$ signal and the NCN6804 related functions are updated accordingly.

NCN6804
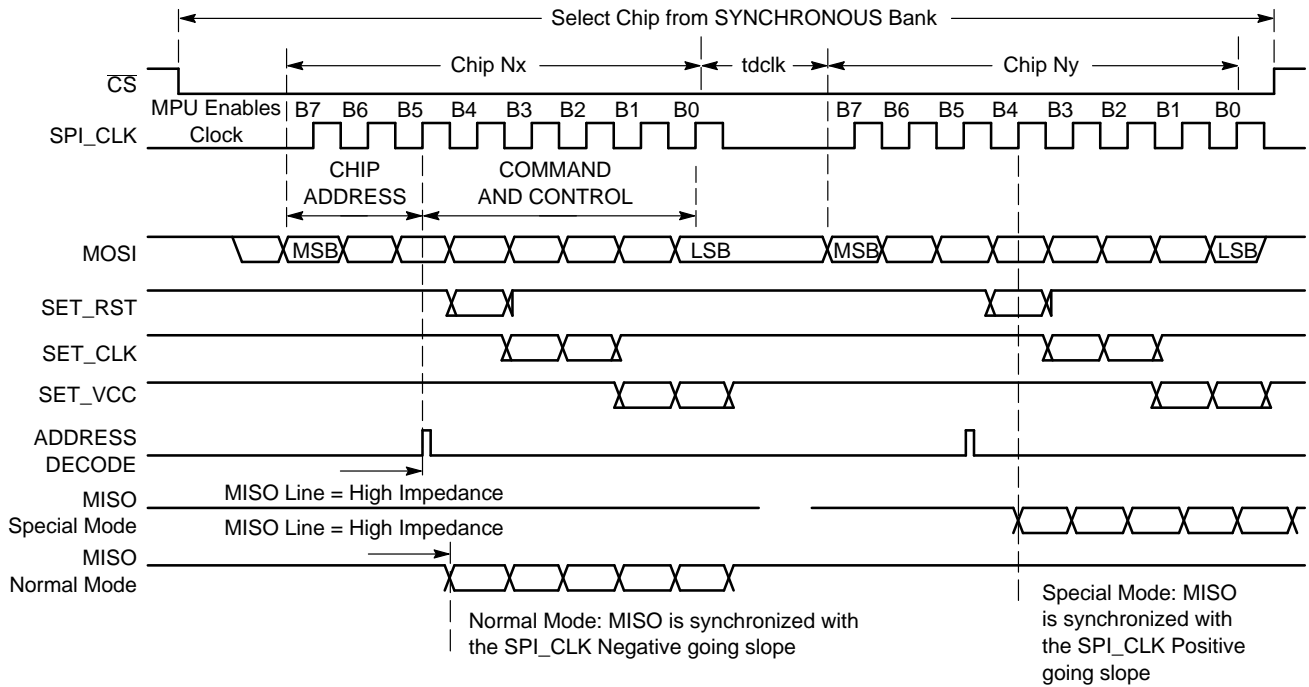
Figure 13. Basic Multi Command SPI Bytes

Since the 2 dual circuits present in the Asynchronous Bank have an individual physical address, the system can control 2 of these chips by sending the data content within the same $\overline{CS}$ frame as depicted in Figure 13. The bits are decoded on the fly and the related sub blocks are updated accordingly. According to the SPI general specification, no code or activity will be transferred to any chip when the $\overline{CS}$ is High.

When 2 SPI dual bytes are sequentially transferred on the MOSI line, the CLK_SPI sequence must be separated by at least one half positive period of this clock (see td$_{clk}$ parameter).

The oscillograms given Figures 14 and 15 illustrate the SPI communication protocol.
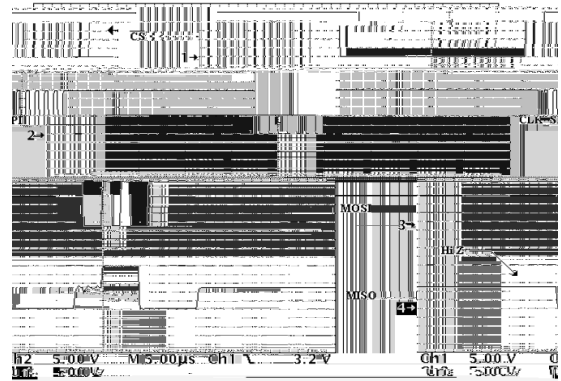
Figure 14. Programming Sequence

Special mode

Standard mode
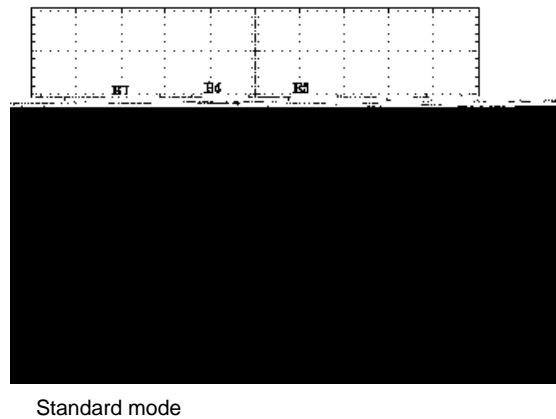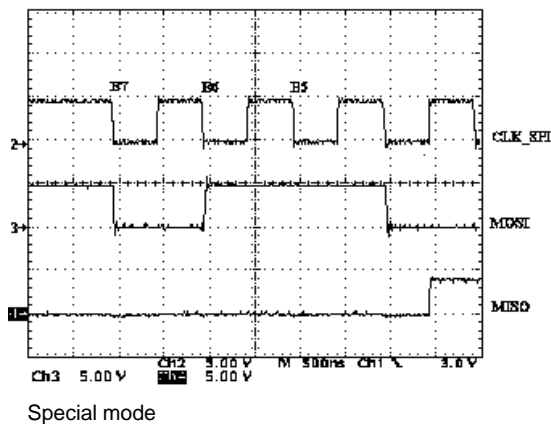
Figure 15. MISO Read Out Sequences

CRD_VCC Charged

Figure 17. Theoretical DC/DC Operating Waveforms
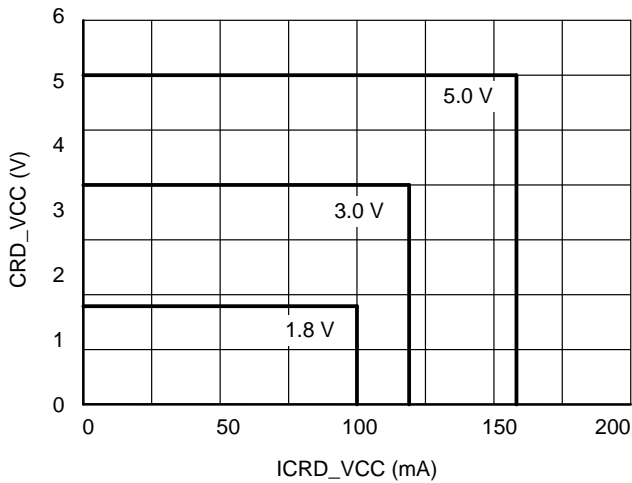
Figure 20. Output Current Limit: Output voltage CRD_VCC (1.8 V, 3.0 V, 5.0 V)

On the other hand, the circuit is designed to make sure no over current exist over the full temperature range. As a matter of fact, the output current limit is reduced when the temperature increases.

DC−TO−DC Converter External PASSIF Component Selection

To be functional the NCN6804's DC to DC converters need external passive components carefully selected. The performance and specification compliance of the NCN6804 are guaranteed by the DC/DC converter input capacitor, by the inductor and the reservoir capacitor characteristics. The input capacitor enables the decoupling and filtering of the input power supply voltage (V_{BAT}) and its value has to be high enough to guarantee a good operating stability of the converter. A CMS very low ESR capacitor shall be preferably used with a minimum value of 4.7 μF recommended, 10 μF will be preferred   this will strongly depend on how the capacitance value varies with the DC voltage applied across the capacitor terminals (see Figure 21). The inductor shall be sized to handle the 500 mA peak current (Min. I_{sat}) flowing during the DC/DC operation and will have to offer a low parasitic series resistor in order to maintain a good efficiency (Ex:108PS 3.8142 0 TD0 Tc<00ef Fj/TT7 1 Tf.5886 0 TD−0306 Tc.1754 (lpowert hae 5 om

NCN6804

CLOCK_IN ∏∏∏∏∏∏∏∏∏∏∏∏

CLOCK : 2 ⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔⊓⊔ Internal

CLOCK : 4 ⊓⊔⊓⊔⊓⊔⊓⊔

B2 ─────────────

These bits program
CLOCK = 1:1 ratio

B3 ─────

Clock is updated upor

CRD_CLK ⊓⊔⊓⊔∏∏∏∏∏

CLOCK programming is activated
by the B2 + B3 logic state
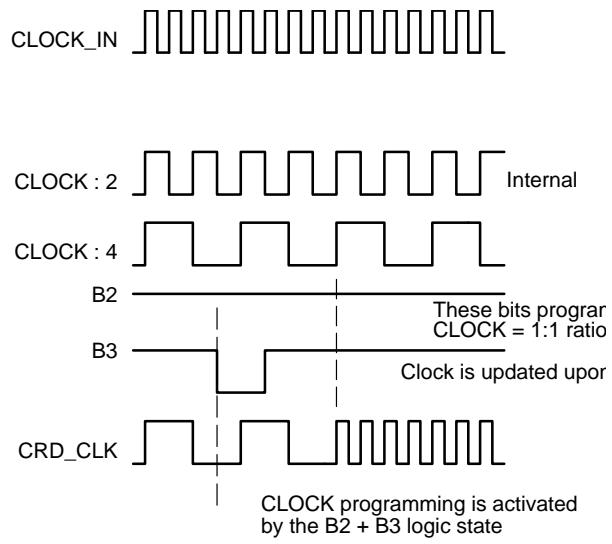
Input Schmitt Triggers

All the Logic Input pins have built in Schmitt trigger circuits to protect the NCN6804 against uncontrolled operation. The typical dynamic characteristics of the related pins are depicted Figure 24.
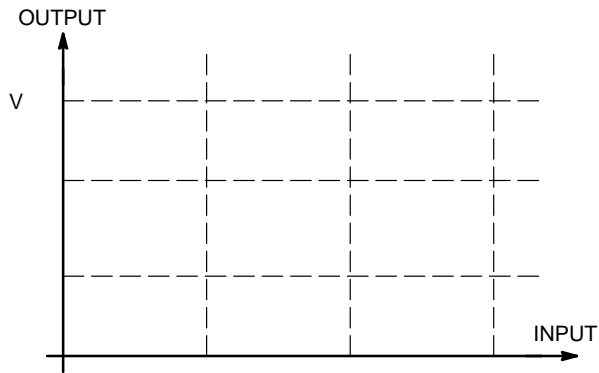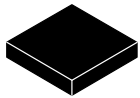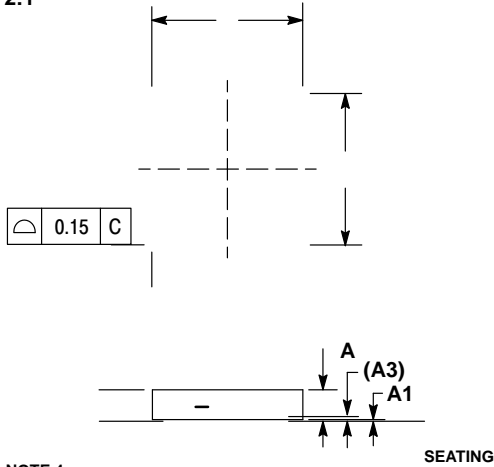

Figure 24. Typical Schmitt Trigger Characteristic

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013

SCALE 2:1

| 0.15 | C |

A
(A3)
A1

NOTE 4

SEATING

		MAX
	0.80	1.00
A1	———	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	———
L	0.30	0.50
L1	———	0.15

D2 → ← K

9
17
1
32

b
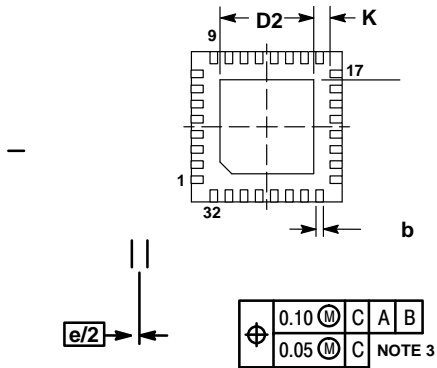
XXXXXXXX
XXXXXXXX
AWLYYWW▪

▪Free indicator, "G" or

| e/2 |

⊕	0.10 Ⓜ	C	A	B	
	0.05 Ⓜ	C			NOTE 3

RECOMMENDED
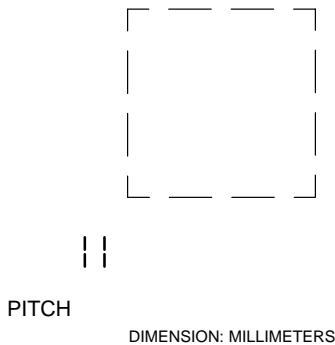
PITCH

DIMENSION: MILLIMETERS

DOCUMENT NUMBER:	98AON20032D	